WT - QTSD

8-Pin Quadrature convertor SOSC (System On Chip Solution)

Description:

The integrated circuit comprises a high speed signal processor and convertor system with input / output protection and conditioning. Quadrature signals presented to the input port are shaped and converted to discrete step and direction terms at the output port at X1 rate. The STEP polarity is pin selectable and can be changed on-the-fly.

Features:

- Complete SOCS (System On Chip Solution)
- Can be used with NO additional components *
- Low-Power Brown-out Reset (BPR)
- Dual mode operation
- Schmitt trigger inputs.
- High power outputs

Functions:

- Conversion of quadrature signals to X1 discrete step and direction.

Operating Characteristics:

- Operating Speed :
  - DC – 20KHz signal input
  - DC – 20 KHz step pulse output
- Step pulse output width :
  - 3uS minimum
- Input level switching :
  - High = $4.5V \leq V_{DD} \leq 5.5V$
  - Low = $1.8V \leq V_{DD} \leq 4.5V$
- Operating Voltage Range:
  - 2.3V to 5.5V (see specifications *)
- Temperature Range:
  - Industrial: -40°C to +85°C
- Internal input clamping
- Output source/sink capability 10ma

**Power supply must meet full specifications as per Electrical Specification page.*

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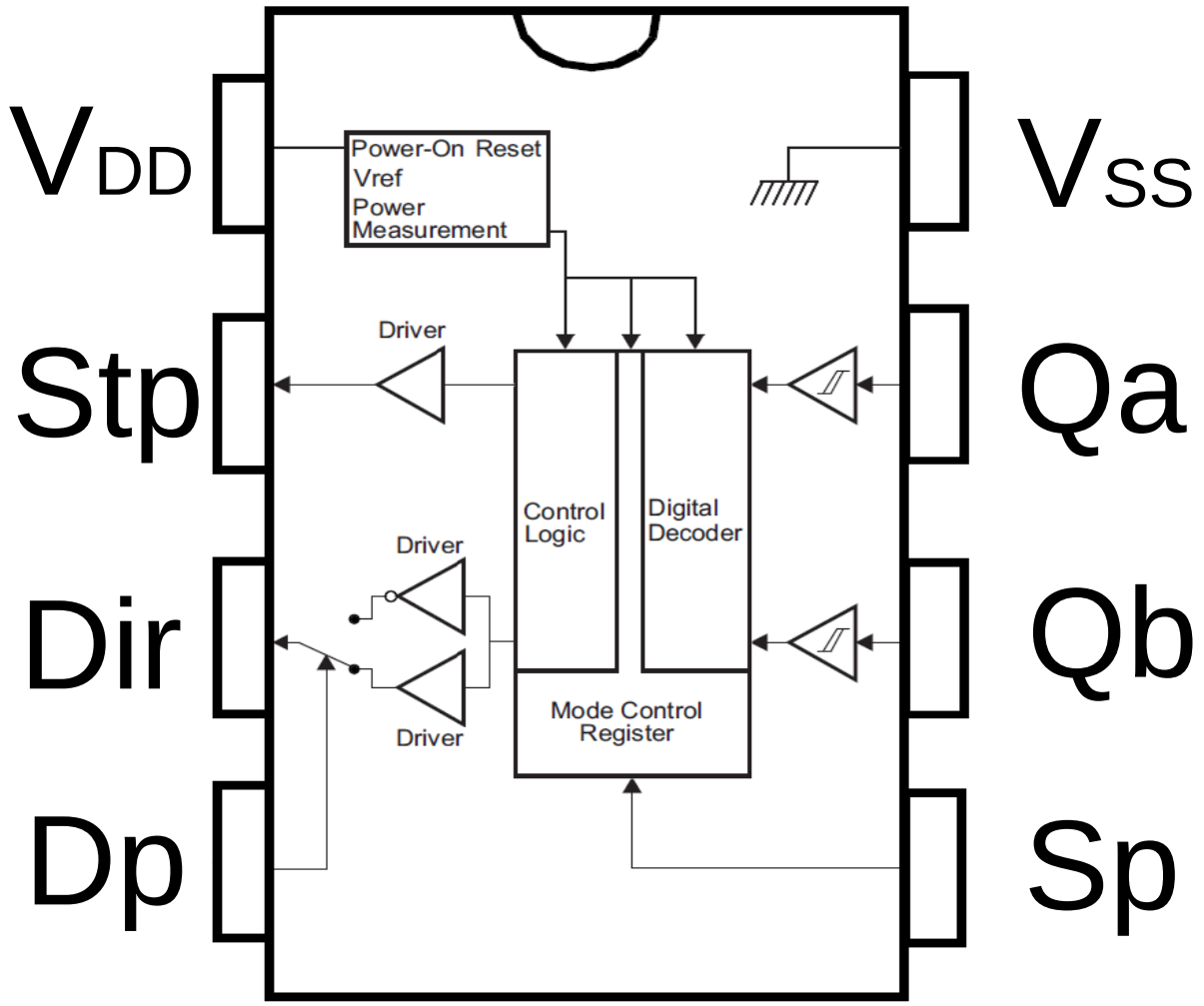
dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions.

PIN DIAGRAM

Pin Diagram – 8-Pin PDIP, SOIC

Fig 1



PIN	Direction	NAME	FUNCTION
1	input	V_{DD}	Vdd, supply input
2	output	Stp	Step pulse output
3	output	Dir	Direction signal output
4	input	Dp	Step pulse polarity selection
5	input	Sp	Direction polarity selection
6	input	Qb	Quadrature signal phase Qa
7	input	Qa	Quadrature signal phase Qb
8	output	V_{SS}	Vss, ground

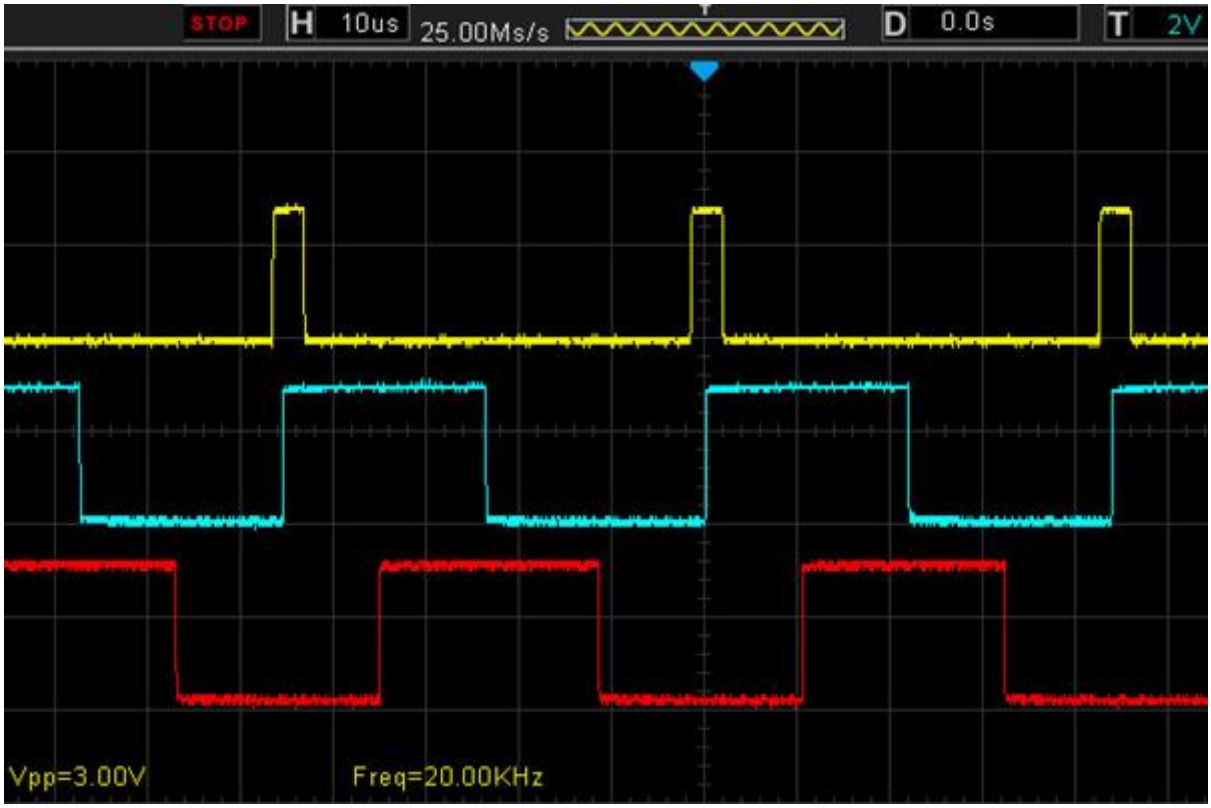
Quadrature input decode correlation to Step output

Quadrature signals presented to the input port are sampled at every rising edge on the Qa input pin which results in a step at every rising Qa edge. A level change will produce a Step pulse of >3 µS. When the quadrature signal reverses (shown below) there will be a delay of about 5µS which is the Direction setup time during which the device will delay the Step pulse. This is necessary for the driver to prepare for a direction change.

Therefore any direction change will cause the next step pulse to be delayed by the setup time.

As the quadrature input signal is sampled at every rising edge of one of the Q inputs, the step pulse (shown in YELLOW below) will be the same frequency as the Q input. Thus a 10 KHz quadrature input (measured on either Qa or Qb) will produce a 10 KHz step pulse output..

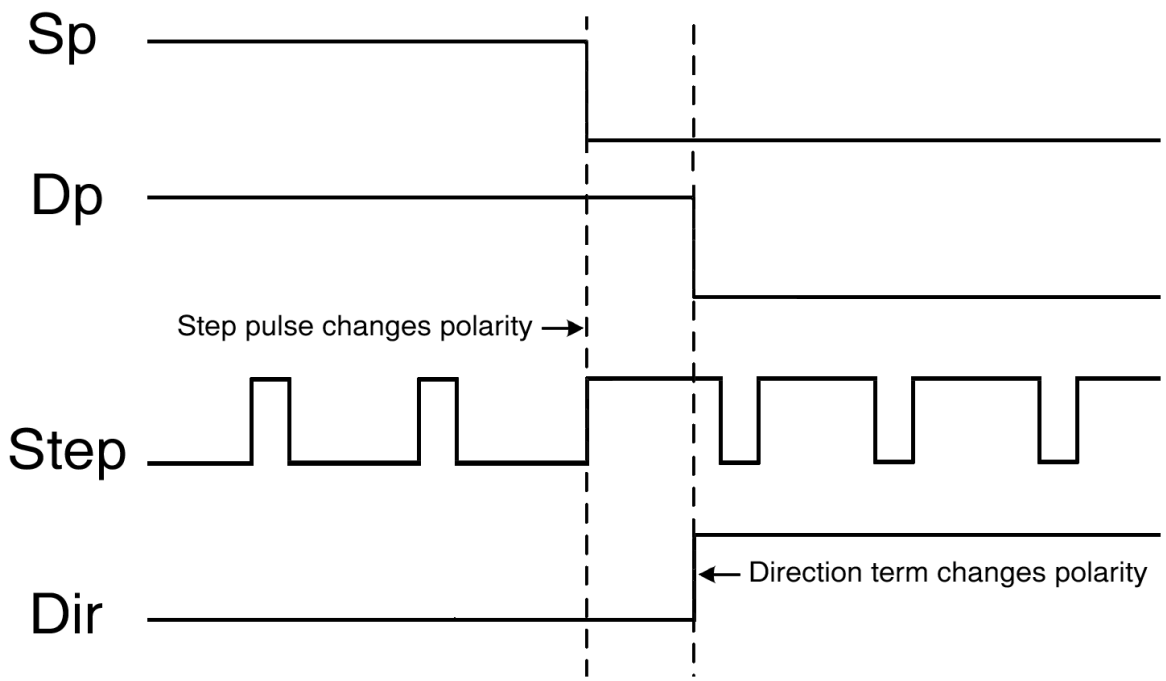
Fig 2



Step and Direction polarity correlation to Step and Direction output

The step and direction outputs can be inverted by tying them to V_{SS} (ground). The diagram in figure 3 shows how the Step and Direction polarity selections affect the Step and Direction output pulses. The Sp and Dp pins have internal pull-ups to prevent spurious outputs when the inputs are floating, this means that their default state ensures that the Direction and Step pulses are active high.

Fig 3

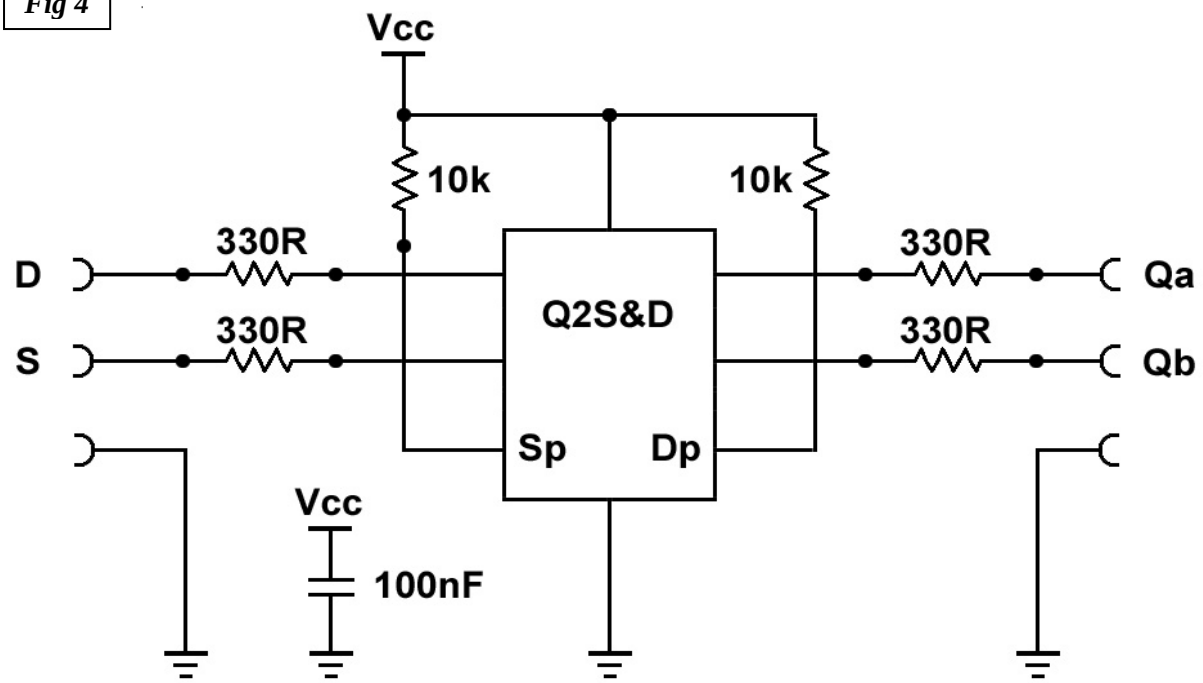


Please note that by design, the Step pulses after the direction change are delayed by the Setup period.

Application notes

Although this device is able to function with no external components it is recommended to have limiting resistors on the inputs and outputs, and a decoupling capacitor positioned close to the V_{SS} and V_{DD} pins. The schematic in figure 4 shows the recommended minimum configuration.

Fig 4



By using 1K resistors in series with the Qa and Qb inputs it is possible to apply a 12vdc input signal with ease. Generally speaking the inputs to most motor drivers will be TTL compatible, which means that very little current is required to switch correctly. The input pins of this device are designed to withstand clamp currents of up to 10mA, therefore the use of 1k resistors on the Step and Direction output pins is adequate.

Remember to consider that the input and ouput pin capacitance will have an effect on rise times.

Should higher current drive capability be required from the output of the circuit in figure 4, simply lower the resistance as needed. It is important that you ensure that the device is not forced to operate in conditions outside of the absolute maximums stipulated in the ELECTRICAL SPECIFICATIONS section within this document.

Note also that there are 10k pullup resistors connected to the SP and SD pins. This is the accepted method of dealing with unconnected pins on this device, even though they have internal pullups, and increases the level of noise immunity.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Ambient temperature under bias.....-40°C to +125°C
Storage temperature ..... -65°C to +150°C
Maximum input frequency..... 20KHz
Voltage on pins with respect to V_{SS}:
On V_{DD} pin..... -0.3V to +6.0V
On all other pins..... -0.3V to (V_{DD} + 0.3V)
Maximum current:
On V_{SS} pin **(1)**
-40°C ≤ T_A ≤ +85°C ..... 80 mA
+85°C ≤ T_A ≤ +125°C ..... 50 mA
On V_{DD} pin **(1)**
-40°C ≤ T_A ≤ +85°C..... 100 mA
+85°C ≤ T_A ≤ +125°C..... 85 mA
Sunk by any output pin..... 10 mA
Sourced by any output pin..... 10 mA
Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) ..... ±10 mA
Total power dissipation.....400 mW
Output low condition……0.6V
Output high condition…… V_{DD} - 0.7V
Capacitive loading on all pins……50pF
Output low condition……0.6V
Internal pull-up current……300 µA

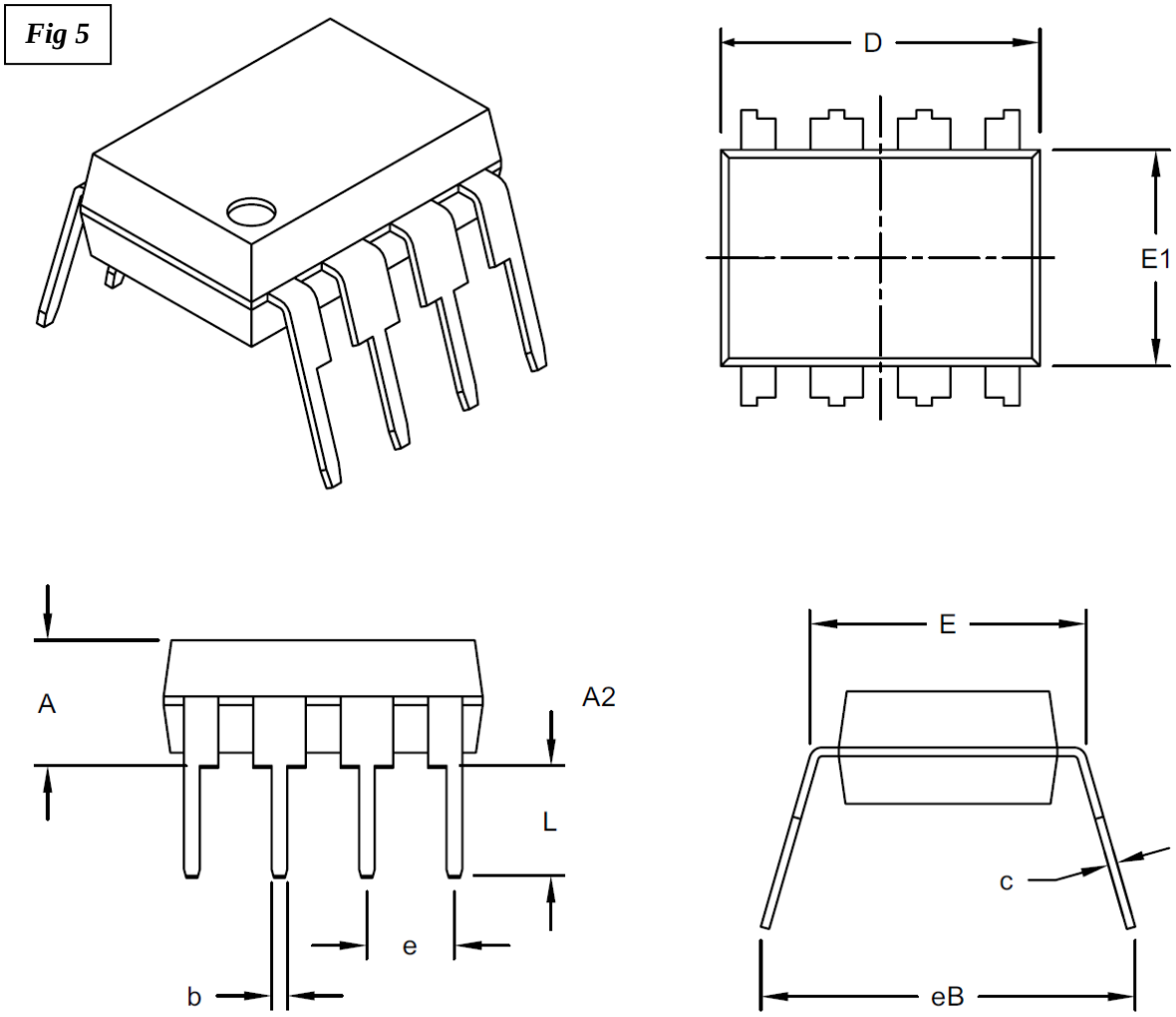
Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be Limited by the device package power dissipation characterizations, see “Thermal Characteristics” to calculate device specifications.

† IMPORTANT NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

Package information

8 lead PDIP (300mil)

Fig 5



Datum	Dimension specifics	imperial inches		
Identifier		Min	Nom	Max
D	Overall Length	.348	.365	.400
E1	Package Width	.240	.250	.280
A	Top to Seating Plane	-	-	.220
A2	Package Thickness	.115	.130	.195
L	Tip to Seating Plane	.115	.130	.150
b	Lower Lead Width	.014	.018	.022
e	Pitch		.100	
E	Shoulder to Shoulder Width	.290	.310	.325
eB	Overall Row Spacing	-	-	.430
c	Lead Thickness	.008	.010	.015

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